

## REMARKS

In the Office Action dated 10/6/03, the Examiner objected to the Abstract. The Examiner also objected to claims 27, 29, 32, 33, 35, and 38 for various informalities. Claims 27-38 were rejected under 35 U.S.C. § 103(a) as being obvious over USP No. 6,295,634 issued to Hiroyuki 5 Matsumoto (hereinafter referred to as “Matsumoto”) in view of USP No. 5,587,923 to Deborah C. Wang (hereinafter referred to as “Wang”). In this Amendment, Applicants have amended the Abstract and claims 27, 29, 32, 33, 35, and 38 in response to the Examiner’s objections. Claims 27 and 33 have also been amended to clarify the subject matter recited therein. New Claims 10 39 and 40 have been added. No new matter has been added. Accordingly, claims 27-40 will be pending after entry of this Amendment.

### **I. Objections to the Abstract**

In the Office Action, the Examiner objected to the language and format of the Abstract. Applicants have replaced the previous Abstract with the Abstract recited above on page 5 of this Amendment. Applicants believe this new Abstract addresses the Examiner’s concerns and 15 therefore respectfully request withdrawal of the Examiner’s objection to the Abstract.

### **II. Objections to the Claims**

In the Office Action, the Examiner objected to claims 27, 29, 32, 33, 35, and 38 for various informalities. Except as discussed below with respect to claim 27, Applicants have amended these claims in accordance with the Examiner’s requirements. Accordingly, Applicants 20 respectfully request withdrawal of the objections to claims 27, 29, 32, 33, 35, and 38.

Applicants respectfully disagree with the Examiner’s assertion that the word “costs” in line 10 of claim 27 should be changed to the word “cost”. According to the preamble of claim 27, “a plurality of edges exist between said sub-regions” (emphasis added). Claim 27 further recites that “an edge-intersect cost” is identified “for each particular edge”. Because the word

“costs” indirectly refers to the word “edges” recited in the preamble, the word “costs” should be plural. Applicants have therefore not changed the word “costs” in line 10 of claim 27 to the word “cost” as the Examiner has required.

### **III. Rejection of the Claims Under 35 U.S.C. § 103(a)**

5 In the Office Action, the Examiner rejected claims 27-38 under 35 U.S.C. § 103(a). The Examiner stated that the claimed invention was obvious over Matsumoto in view of Wang. Applicants respectfully submit that the combination of Matsumoto and Wang does not render any of claims 27-38 obvious for at least the following reasons.

To establish a *prima facie* case of obviousness, the prior art reference (or references when 10 combined) must teach or suggest all the claim limitations. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Next, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000).

#### **15 A. Claims 27-32**

Applicants respectfully submit that the combination of Matsumoto in view of Wang does not identically describe every step of claim 27 because neither Matsumoto nor Wang, alone or in combination, describe either a step which entails:

20 for a first set of sub-regions wherein each sub-region of the first set includes a contact point, identifying a first set of potential routes, wherein each route in the first set of potential routes traverses the first set of sub-regions through the contact point of each sub-region of the first set

or a step which entails “for each particular edge, identifying an edge-intersect cost that is 25 dependent on the number of routes in the first set of potential routes that intersect the particular edge” as recited in amended claim 27.

Matsumoto describes a method for designing wiring for connecting bonding pads of a semiconductor chip to pins provided on a semiconductor package wherein the semiconductor package surrounds the semiconductor chip. Col. 5, line 65-Col. 6, line 7. The method entails utilizing Delaunay triangulation to ensure illegal wiring conditions referred to as crossings and 5 detourings do not occur. Col. 6, lines 4-7. The triangulation process entails dividing a wiring plane of the semiconductor package into a plurality of virtual triangles wherein each triangle has a pin and a bonding pad as apexes. Col. 6, line 9-12. In contrast, the present invention provides a method for pre-computing attributes of net routes. The method entails identifying a first set of routes wherein each of the first set of routes traverses through a contact point included within 10 each sub-region of a first set of sub-regions. Next, the method identifies an edge-intersect cost for each particular edge between sub-regions wherein the edge-intersect cost is dependent upon the number of routes in the first set of potential routes that intersect the particular edge. Finally, the identified edge-intersect costs are stored.

The Examiner asserts that the dashed lines between pins 0, 1, 2, and 3 in Figure 18 of 15 Matsumoto describe the first set of potential routes recited in the identifying step of claim 27. Applicants respectfully disagree. These triangular regions of Figure 18 are not described as each having a contact point and the routes the Examiner identifies do not each traverse the contact point within each triangular region. None of the routes illustrated in Figure 18 have a single point in common as they traverse within any one of the triangular regions. In fact, each of these 20 routes utilizes a completely independent set of points within each triangular region that each route traverses.

In addition to failing to identically describe the step of identifying routes as recited in claim 27, Matsumoto also fails to identically describe the step of identifying an edge-intersect cost for each particular edge as recited in claim 27. The Examiner admits to this fact in the

Office Action, but asserts that Wang makes up for this deficiency. Applicants respectfully submit that Wang does not make up for this Matsumoto deficiency and, even if Wang did make up for this deficiency, there is not motivation for combining the teachings of Matsumoto and Wang.

5           Wang describes a cell placement for a microelectronic integrated circuit. Abstract. The Examiner asserts that the edge capacity concept described in Wang at Col. 8, lines 22-27 describes the edge-intercept cost recited in claim 27. However, the section of Wang the Examiner cites discusses how a porous edge will allow more wires to go through than a non-porous edge will allow. The concept the Examiner cites in Wang identifies the potential for an 10 edge to accommodate a number of wires. Wang does not describe determining the ability of an edge to allow a predetermined specific number of wires to pass through. Nothing in Wang describes first identifying a particular set of routes and then identifying an edge-intersect cost for each particular edge wherein the edge-intersect cost is dependent on the number of routes in the first set of identified potential routes that intersect the particular edge. Accordingly, Wang does 15 not identically describe the edge-intercept cost identifying step recited in claim 27.

          In addition to the above, Applicants respectfully submit that there is no motivation for combining the teachings of Matsumoto and Wang. The Federal Circuit in In re Katzab, supra, requires that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or 20 to combine reference teachings. Nothing in Matsumoto or Wang suggests or motivates combining their teachings. Further, Applicants are unaware of any knowledge available to one skilled in the art which would suggest or motivate combining Matsumoto and Wang. If the Examiner believes that this knowledge is available to one of ordinary skill in the art, the Examiner is requested, in accordance with MPEP §2144.03, to provide a reference or references

supporting all of the features the Examiner believes are “well known”. If the rejection is based on facts within the personal knowledge of the Examiner, the Examiner is requested to support the rejection with an affidavit setting forth the facts upon which the Examiner’s rejection is based. See 37 C.F.R. 1.104(d)(2). Applicants should be given an opportunity to address the new 5 reference(s) or affidavit.

Because the combination of Matsumoto and Wang fails to identically describe both the “identifying” steps of claim 27, this combination does not identically describe each step of claim 27. Accordingly, Applicants respectfully submit that Matsumoto in view of Wang does not render the subject matter of claim 27 obvious. Applicants therefore respectfully request 10 withdrawal of the rejection of claim 27 under 35 U.S.C. § 103(a) as anticipated by Matsumoto in view of Wang.

Each of claims 28-32 are dependent, either directly or indirectly, upon independent claim 27. Therefore, claims 28-32 are patentable over the combination of Matsumoto and Wang for the same reasons that independent claim 27 is patentable over the combination of Matsumoto and 15 Wang.

## **B. Claims 33-38**

Applicants respectfully submit that Matsumoto in view of Wang does not identically describe every step of claim 33 because neither Matsumoto nor Wang, alone or in combination, describe either a step which entails “for a first set of sub-regions wherein each sub-region of the 20 first set includes a contact point, identifying a first set of potential routes that traverse the first set of sub-regions through the contact point of each sub-region of the first set” or a step which entails “for each particular path, identifying a path-use cost that is dependent on the number of routes in the first set of potential routes that use the particular path” as recited in amended claim 33. As mentioned above, Matsumoto describes a method for designing wiring for connecting

bonding pads of a semiconductor chip to pins provided on a semiconductor package wherein the semiconductor package surrounds the semiconductor chip. Claim 33 recites a step of identifying a first set of potential routes which is identical to this same step as recited in claim 27. Thus, for the same reasons discussed above with respect to claim 27, Applicants submit that Matsumoto 5 does not identically describe this identifying step recited in claim 33.

Applicants respectfully submit that Matsumoto also fails to identically describe the step of identifying a path-use cost as recited in claim 33. The Examiner admits to this fact in the Office Action, but asserts that Wang makes up for this Matsumoto deficiency. Applicants respectfully disagree. The path-use identification step recited in claim 33 is similar to the edge-10 intersect cost identifying step recited in claim 27. In fact, the Examiner cites the reasoning he applied to this similar step in claim 27 to support his assertion that Wang describes this step of claim 33. Thus, for reasons identical to the reasons Applicants discussed above with respect to the edge-intersect cost identifying step of claim 27, Applicants submit that Wang does not identically describe the path-use identification step of claim 33.

15 Because the combination of Matsumoto and Wang fails to identically describe both the “identifying” steps of claim 33, this combination does not identically describe each step of claim 33. Accordingly, Applicants respectfully submit that Matsumoto in view of Wang does not render the subject matter of claim 33 obvious. Applicants therefore respectfully request withdrawal of the rejection of claim 33 under 35 U.S.C. § 103(a) as anticipated by Matsumoto in 20 view of Wang.

Each of claims 34-38 are dependent, either directly or indirectly, upon independent claim 33. Therefore, claims 34-38 are patentable over the combination of Matsumoto and Wang for the same reasons that independent claim 33 is patentable over the combination of Matsumoto and Wang.

#### **IV. New Claims 39 and 40**

In this Amendment, Applicants have added new Claims 39 and 40. Applicants respectfully submit that these new claims are patentable over Matsumoto in view of Wang because this combination of references fails to disclose, teach, or even suggest the limitations in 5 these claims. The limitations of claims 39 and 40 are similar to the limitations of claims 27 and 33, respectively, except for the additional limitation in each of claims 39 and 40 that at least two routes are identified. Because the combination of Matsumoto and Wang does not identically describe both these “identifying” steps without the at least two routes limitation (as discussed above) it follows that this combination of references also does not identically describe these steps 10 when the additional limitation of at least two routes is included within the recitation as in claims 39 and 40.

#### **V. Information Disclosure Statement**

Accompanying this Amendment is a 1449 form of an Information Disclosure Statement that Applicants are submitting concurrently with but separately from this Amendment. This 15 Information Disclosure Statement lists and provides copies of several additional references for the Examiner's consideration. The Examiner is requested to make these documents of record. Also attached is a second group of 1449 forms of Information Disclosure Statements that Applicants have submitted prior to submission of this Amendment but which Examiner has not yet made of record. The Examiner is requested to make these documents of record as well.

## CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 27-40, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

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Respectfully submitted,

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